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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/058,005	01/29/2002	Kenji Suzuki	100353-00096	3133

7590

07/03/2003

ARENT FOX KINTNER PLOTKIN & KAHN, PLLC
Suite 600
1050 Connecticut Avenue
Washington, DC 20036-5339

EXAMINER

IM, JUNGHWA M

ART UNIT

PAPER NUMBER

2811

DATE MAILED: 07/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/058,005

Applicant(s)

SUZUKI ET AL.

Examiner

Junghwa M. Im

Art Unit

2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 18 April 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1, 3, 10 and 11 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1, 3, 10 and 11 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 1.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 102/103

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in-

(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or

(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

Claims 1, 3 and 11 are rejected under 35 U.S.C. 102(e) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Bassett (U.S. Pat. No. 6,242,814).

Regarding claims 1 and 3, Fig. 7 of Bassett shows a semiconductor integrated circuit comprising:

Pads (40's), a first power supply I/O cell (one of 40's, a second Vdd to the right) which is connected by a wire (210) to an external pin through a corresponding one of said pads, a second power supply I/O cell (one of 40's, a first Vdd to the right) which is not connected by a wire 210 to an external pin through a corresponding one of said pads, but receives power supply from said first power supply I/O cell, an internal cell (150 in Fig. 4; a logic cell) and a power supply line (Vdd 50 in Fig. 3) which provides power supply to the internal cell wherein the first power supply I/O cell and the second power supply I/O cell are connected to the power supply line.

It is quite evident that power is provided to an internal cell through a power supply line for the device to operate functionally. In detail, Bassett shows in Fig. 3 a plurality of Vdd pads

Art Unit: 2811

40's as a Vdd line 50 and Fig. 4 shows all Vdd pads are connected to a power supply of the active circuitry 140 through contact layer 130 (col. 3, lines 34-56). In addition, Bassett discloses that each of Vdd pads are connected and placed directly over the Vdd bus, thus both the used Vdd cell and unused Vdd cell are connected together through one of the bus line. And the bus is connected to a corresponding band pad site for the power supply, thus the unused Vdd cells receives power through the wire connected Vdd cell which is connected to the Vdd bus together with the unused Vdd cell.

Regarding claim 11, Fig. 7 of Bassett shows a semiconductor integrated circuit comprising pads (40's), a first power supply I/O cell (one of 40's, a second Vdd to the right) which is connected by a wire (210) to an external pin through one of the pads, a second power supply I/O cell (one of 40's, a first Vdd to the right) which is not connected to an external pin (210) through a pad and connected to the first power supply I/O cell through a bus line (col. 3, lines 34-56), an internal cell (150 in Fig. 4; a logic cell), and a power supply line which provides power supply connected to the first power supply I/O cell and the second power supply I/O cell and the internal cell

Claim 10 is rejected under 35 U.S.C. 102(e) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Lin (U.S. Pat. No. 6,246,122).

Regarding claim 10, Lin shows throughout the Figures especially in Fig. 2 a semiconductor integrated circuit comprises: an I/O cell (24) having no external connection, and assigning the identified I/O cell to be a power supply I/O cell having no external connection.

Art Unit: 2811

Lin shows that an unused I/O cell which is not in use and thus is not connected to an I/O pin (referred as an NC pin, a no-connected pin). Lin shows in Fig.2 a no-connect pin (24) which corresponds to an unused I/O cell without an external connection, and this NC pin is connected through bond pad (22) to EDS protective unit (23) which can work as a power supply.

Note that the preamble recites a product by process limitation. Even though product by process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product by process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process. *In re Thorpe*, 777F. 2d 695,698 UPSQ 964,966 (Fed. Cir. 1985).

Response to Arguments

Applicant's arguments filed on April 18, 2003 have been fully considered but they are not persuasive.

On page 4, Applicant argues that Basset does not teach a first and a second power supply I/O cells (a first Vdd pad and a second Vdd pad) are connected to a power supply line provided to an internal cell. First, Basset device has an internal cell which is a logic cell. Therefore, it is inherent that there is a power supply line to the internal cell to provide power for operating the device. Without adequate power supply, the device will not operate. Second, as discussed above in the rejection, Bassett discloses that both of the first power supply I/O cell and the second power supply I/O cell are connected together through the power supply bus line (Vdd bus

Art Unit: 2811

line) to a corresponding power supply bond pad site. More specially, Figure 3 shows a power line Vdd 50 connecting each Vdd pad.

In response to applicant's argument regarding Claim 10, the I/O cell connected to the pin would read on the power supply I/O cell since the pin is connected electrically to power bus. Note that claim 10 requires an I/O cell with no external connection, which is shown as an NC pin which receives a signal (col. 3, line 36), and can be identified to be a power supply I/O cell.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

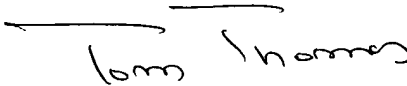
Art Unit: 2811

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junghwa M. Im whose telephone number is (703) 305-3998. The examiner can normally be reached on MON.-FRI. 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

JMI
June 25, 2003


TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800